Aurora/Aurora+ IMU

E2E paper

https:// www.imems-technology.com

What is an IMU:

- **IMU (Inertial Measurement Unit).**
- **IMU uses basically 3 accelerometers and 3 gyroscopes.**
- **The IMU is designed to perform the following tasks:**
  - Measure Euler angles. **Roll, Pitch, Yaw**, which is three angles that describe the orientation of a rigid body in the space with respect to a fixed coordinate system.
  - linear velocities and the linear accelerations.
  - **Heave Motion** for marine applications.

    Accurate heave measurements are extremely important in the application of marine field to actively compensate for wave motion of a ship.

    Active heave compensation (AHC) systems require an accurate estimate of the vertical vessel motion in order to decouple the offshore crane's lift operation from the motion of the vessel.

    In **Aurora IMU** the heave motion is estimated based on measurements from the accelerometers using an adaptive heave filter. Our custom Field Programmable Gate Array (**FPGA**) guarantees high accuracy and no latency heave estimation.

Why Aurora IMU?

Aurora IMU offers low cost, high accuracy IMU solutions, this was achieved by our **FPGA** & DSP integration in our electronic design.

FPGA offers a whole new level of real time performance and filtering excellence. The platform is taking advantage of real hardware circuitry, allowing extremely low latency measurements and estimation.
With focusing on data processing and noise filtering and not extremely high cost gyroscopes and accelerometers **Aurora has achieved high performance at low cost and small size**.

an advanced distributed parallel calculation algorithm delivers the maximum performance of the unit.

Advantages of FPGA:

FPGA (**Field Programmable Gate Array)** is a re-programmable silicon chips. Using inbuilt logic blocks, lookup tables, builtin DSP units, PLLs and programmable routing resources, one can configure these chips to implement custom hardware functionality such as data filtering, mathematical estimation and communications.

One can develop digital computing tasks in software using **VHDL** programming and compile them down to a configuration file or bit-stream that contains information on how the components should be wired together.

FPGAs provide hardware-timed speed and reliability. Unlike processors, FPGAs are truly **parallel in nature**, so different processing operations do not have to compete for the same resources. Each independent processing task is assigned to a dedicated section of the chip, and can function autonomously without any influence from other logic blocks. **As a result, the performance of one part of the application is not affected when you add more processing.**

Knowing that any IMU needs 3 Accelerometers, 3 Gyroscopes, 3 magnetometer, aiding GPS receiver, and also in each Accelerometer/Gyroscope there is an embedded temperature sensor used to compensate for temperature drift or bias, this means in total there are a minimum of 13 resources of information that needs to be read, filtered for noise removing, and processed to extract the desired output data such as angular position, linear acceleration and linear position, if a typical unit uses a **DSP** processor, reading from all the available sensors is going to be done in series, this means time is lost only for collecting data from the sensors, next step is going to be data filtering, here the system is going to be objected to phase shift, for real time calculation where **phase shift** is not tolerated the mathematical calculation core will not be able to achieve the required accuracy if the quality of signal is low.

Here comes the real problem when it comes to MEMS technology.

The main characteristics of MEMS accelerometers and gyroscopes is the high level of noise, MEMS technology has the huge advantage of reducing the size of accelerometers and gyroscopes, the cost of this reduction is the quality of the signals.

MEMS accelerometers has a very low **Signal-to-noise** ratio, which means a high level of background noise, to overcome this issue, designers have to filter the signal with high order filters, the cost is an increasing none linear **phase shift**, this makes it mission impossible for a signal processing engineer to realize a solution when the system is required to run in Real Time.

The designer may consider additional trade-offs between performance and cost of MEMS sensors, for a very high quality MEMS sensor the cost increases dramatically.

That is why high accuracy MEMS based IMUs are very expensive, the problem is not going to be ended up here, but also it is going to be reflected on the calculation complexity and the execution time, a DSP designer is going to be directed to use high resolution adders, multipliers and division registers in order to achieve the maximum possible accuracy, this is going to extremely increase both the complexity and the execution time of the algorithm, which is already characterized as high complexity algorithm.

Deciding between traditional DSP and FPGA

At high data rates the DSP may struggle to capture, process and output the data without any loss. This is due to the many shared resources, buses and even the core within the processor. **The FPGA, however, is capable of dedicating resources to each of these functions.**

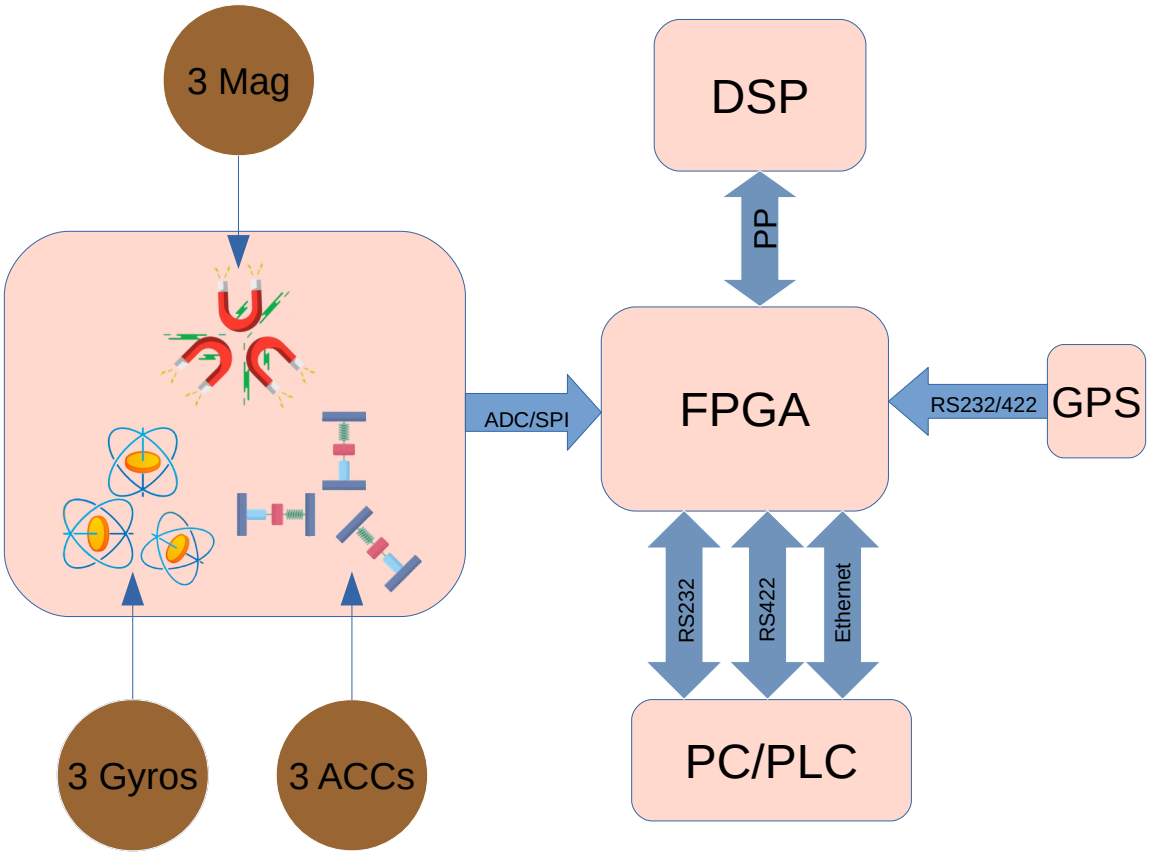
DSPs are instruction based, not clock based. Typically, three to four instructions are required for any **mathematical operation** on a single sample. The data must first be captured at the input, then forwarded to the processing core, cycled through that core for each operation and then released through the output.

In contrast, the FPGA is clock based, so every clock cycle has the potential ability to perform a mathematical operation on the incoming data stream.

Often it is simpler and more efficient to break a high-level system block diagram into FPGA modules and IP cores than mapping it into a C/C++ code for DSP implementation.

Using FPGA, the trade-offs between performance and cost of MEMS sensors is easily biased to low cost MEMS sensors.

Aurora IMU Block Diagram



Aurora IMU is taking full advantage of an **FPGA** based hardware circuitry, allowing for extremely low latency measurements and estimation.

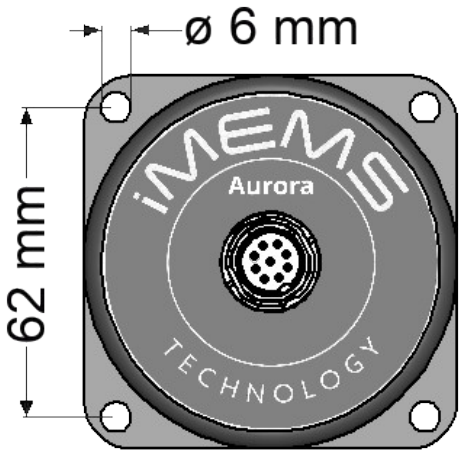
Using FPGA, Aurora has achieved a minimum calculation speed of 1KHZ, and data measuring and estimation of minimum 3KHz.

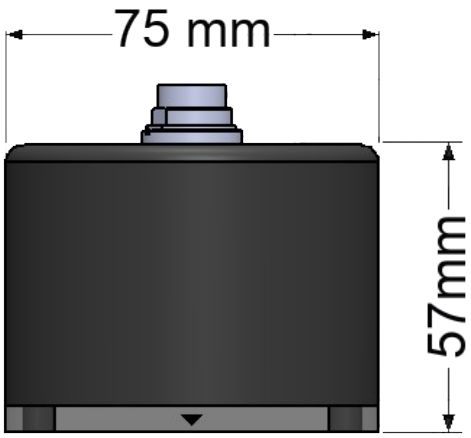
Aurora internal filter runs at minimum speed of 1000Hz and data can also be output at this rate over high speed Serial Port or over Ethernet. its low manufacturing price and great immunity to noise and vibrations makes it the best choice for unstable platforms control.

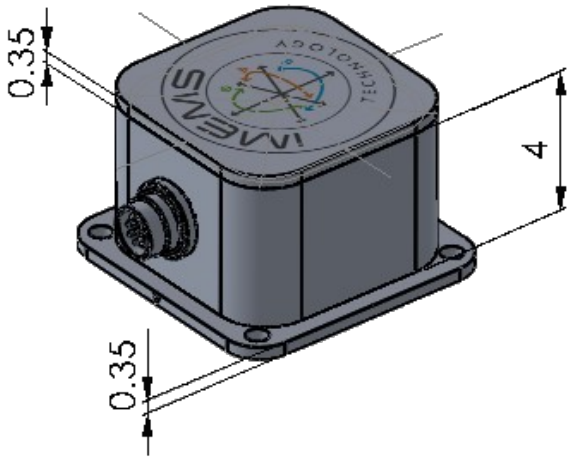
Data filtering, data processing, parameters estimation and communications are realized in a parallel independent logic blocks.

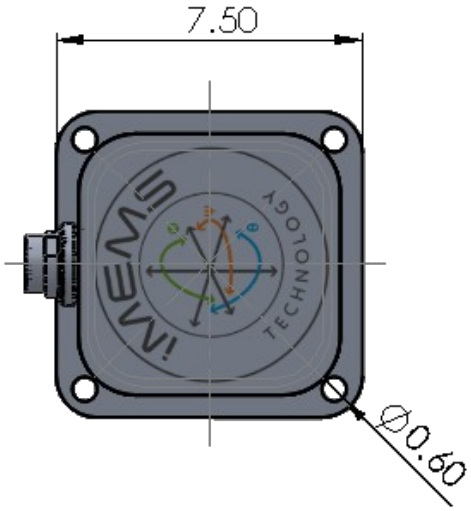
a standard IMU is capable of a 100Hz range calculation speed.

As a result, Aurora has achieved high performance at extreme low cost and very small size.





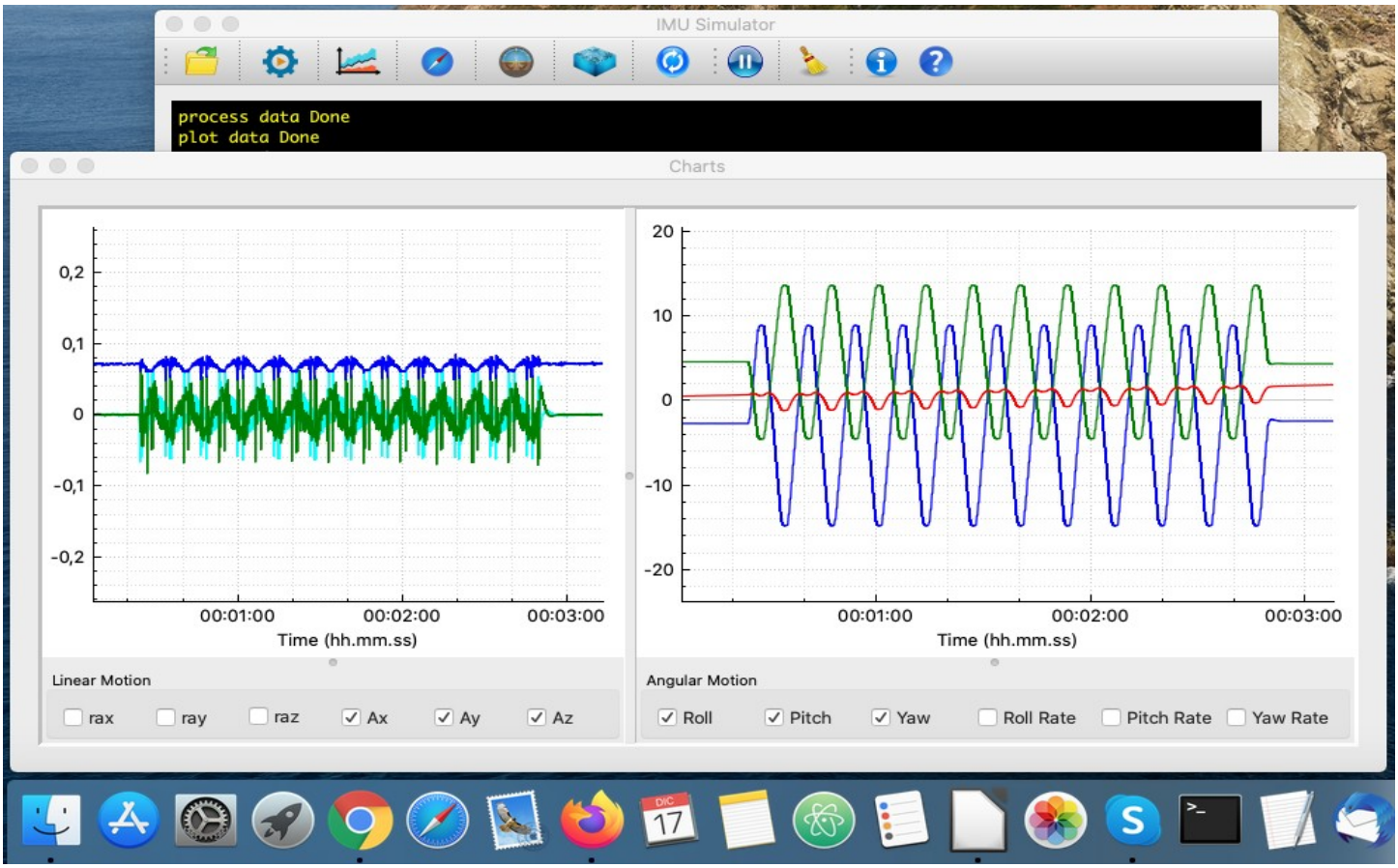




IMU Simulator:

Simulation is a powerful and *important tool* because it provides a way in which designs can be evaluated and tested, iMEMS Technology new technologies and achievements are supported by a real post process simulator, the simulator takes as an input the raw data from the sensor, simulates and models all the mathematical functionality of the IMU to gain insight into their functioning.

The following Figure shows the *simulation* results of a real movement monitored and logged by Aurora IMU. The IMU Simulator *Results* show that the numerical *results* agree well with *experimental* data.



About iMEMS Technology

- Founded in Italy with Innovative ideas, iMEMS Technology designs and produces high end Inertial Measurement Unit **IMU** and **MRU**.
- iMEMS Technology was selected between the most innovative start up companies in the 2019 **Taizhou International Talent Cooperation Fair**, in Taizhou-China while representing the Italian Lazio State *startups*.
- iMEMS Technology was awarded the prize **Premio Best Practices per l'Innovazione** for the year 2019 by the **Confindustria Salerno** Italy.

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